EXHIBIT A

United States Patent [19]

Beasom

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[45] **Date of Patent: Apr. 18, 1989**

[54] **HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION**

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[73] Assignee: Harris Corporation, Melbourne, Fla.

[21] Appl. No.: 831,384

[22] Filed: Jan. 7, 1986

[51] Int. Cl.[4] H01L 29/80

[52] U.S. Cl. 357/22; 357/23.8; 357/35

[58] Field of Search ..... 357/23.8, 22 E, 22 F, 357/22 G, 35

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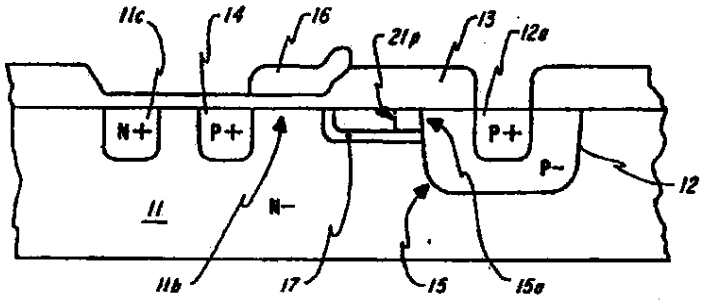
Primary Examiner—Joseph E. Clawson, Jr.

Attorney, Agent, or Firm—William A. Troner; Charles C. Krawczyk

[57] **ABSTRACT**

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

19 Claims, 3 Drawing Sheets



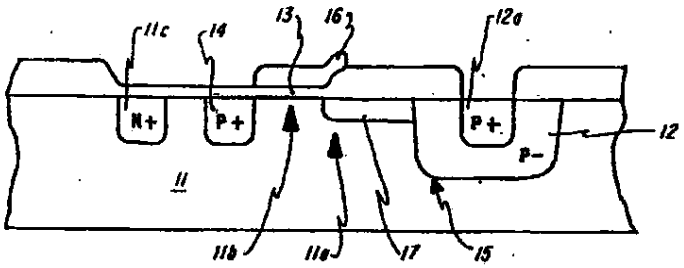


FIG. 1

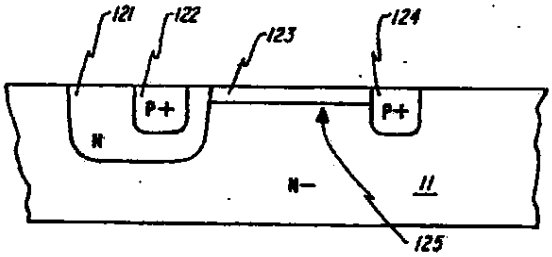


FIG. 2

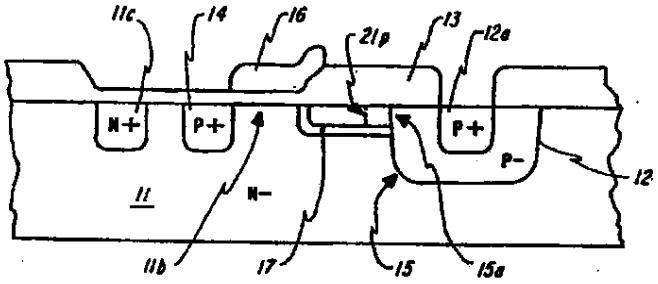


FIG. 3

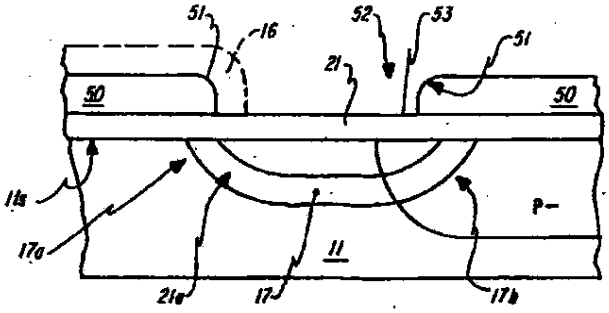


FIG. 4

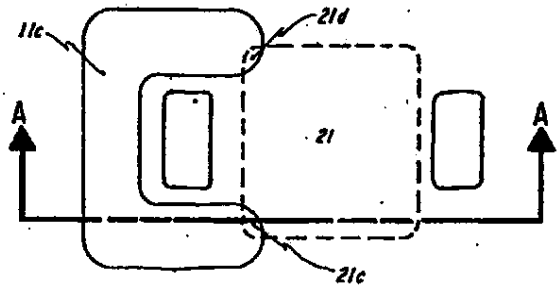


FIG. 5a

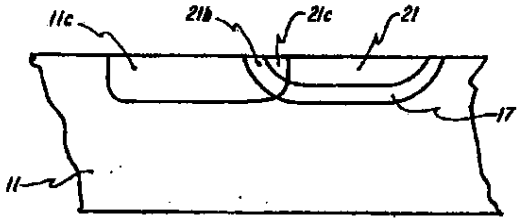


FIG. 5b

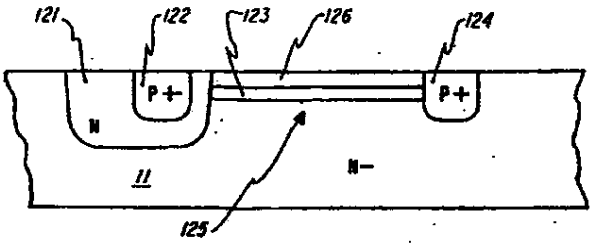


FIG. 6

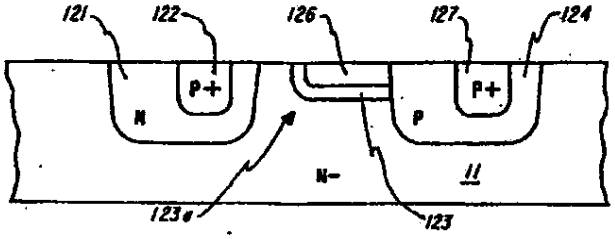


FIG. 7

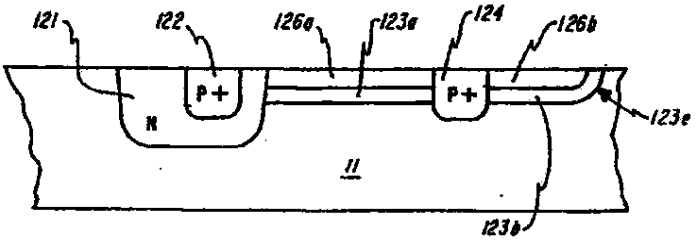


FIG. 8

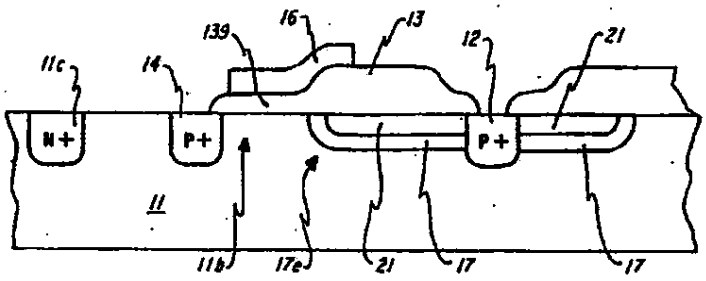


FIG. 9

HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N^{31} substrate 11 and is located so as to lie adjacent the P− drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_c and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel to body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also, the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 2, an N− substrate 11, has an N type emitter shield 121 formed therein and P+ emitter 122 and collector 124 located as shown. Additionally, a P− drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore providing improved frequency response.

At high base collector voltages the drift region, 123, depletes by JFET action with the N-base, 11, and N

shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 3 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 4 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 5*a* and 5*b* are respectively a top view and is a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 6 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 9 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 3 shows an MOS device where P+ drain contact 12*a* is formed in P− type drain 12, P+ source 14 is formed in the N− body 11 and N+ body contact 11_c is provided in the N− body 11. The MOS channel region 11_b is in the N− body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_a of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any non-depleted portion of the top gate does not result in a breakdown of the top

gate to drift region junction. Proper doping of the top gate will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 3 provides reduced ON resistance in the JFET channel relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body to drain breakdown. This is possible because of the provision of the top gate 21. The top gate to channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, results in the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel charge. Thus, for a drift region having a doping of 1×10^{12} boron atoms per square centimeter over the drift region surface in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body to drain voltage of less than the breakdown voltage of the top gate to drain junction 15_b. Since top gate 21 is connected to body 11, the voltage at the top gate to drain junction 15_a will equal the voltage of the body to drain junction 15 voltage and the top gate to drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 should totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 17 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also desirable to insure that the channel of the JFET drift region contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 4 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially effected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and because of the graduated thickness of the implant mask 50 (along the edge 51) the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_f of body 11 beyond the end 21_e of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion implanted into the drift region using the implant mask 50 but at an energy level which results in a shallower ion penetration. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method a diffusion process can be used to bring the JFET channel into contact with the surface 11_e of body 11, and hence insure that the JFET channel will contact the inversion layer MOS surface channel. The lateral drift region 17 and top gate 21 are diffused into the body 11 after initial introduction by ion implant. The doping levels and diffusion times are chosen such that the extremity 17_d of drift region 17 diffuses beyond the end 21_e of the top gate 21 and so that the end 17_e reaches the surface 11_e of body 11. In practice, this approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region and top gate may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 4 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate while the top gate may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 5_a which shows the overlapping of the top gate 21 and the body contact 11_c at overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17 as shown in FIG. 5_b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 5_b shows a cross section of the structure of FIG. 5_a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body

contact 11_c. Thus, so long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 2 may be improved by providing an N type top gate 126 as shown in FIG. 6. In this arrangement the top gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate to drift region depletion layer facilitates pinch-off of the drift region. However, as the base 11 becomes more negative the top gate 126 contributes additional surface exposure to the drift region 123 resulting in lower collector resistance.

FIG. 7 shows an improvement over the arrangement shown in FIG. 6. In FIG. 7 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_e of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 7 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 6 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base to collector breakdown voltage for a PNP device is shown in FIG. 8. In addition to the provision of the N type top gate 126_a over the P− drift region 123_a, the top gate and drift region are enlarged to surround the collector 124 and a curved edge 123_d is provided at the periphery of the enlarged portion 123_b of the drift region. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_e extends to the emitter shield 121 as does the drift region 123_e. The P+ emitter 122 is formed in the N+ type emitter shield.

FIG. 9 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 8. For the MOS device, the P+ drain 12 is surrounded by the P− drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_c which rounds up to the surface of the N− substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 8 and FIG. 9, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 8 and drain in FIG. 9 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. In a semiconductor device of the type including a lateral drift region of a first conductivity type formed in a body region, said drift region serving as a JFET channel, the improvement comprising:

a top gate of a semiconductor material electrically connected to said body region and having a second conductivity type over said drift region to cause depletion of said drift region rom the top upon application of a reverse bias voltage to said device,

wherein said top gate laterally abutts a device region to form a junction and has a surface area doping density such that said top gate becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and

wherein said top gate has a surface are a doping density such that it becomes totally depleted at a reverse bias voltage less than the reverse bias voltage at which said drift region becomes depleted.

2. A semiconductor device as claim 1 wherein said drift region as a tapered peripheral edge.

3. A semiconductor device as claimed in claim 2 wherein said top gate has a lateral expanse bounded by said drift region.

4. A semiconductor device as claimed in claim 3 wherein said top gate has a tapered peripheral edge.

5. A semiconductor device comprising:

a semiconductor body of a first conductivity type;

a first device region of a second conductivity type formed in said body;

a second device region of said second conductivity type formed in said body and separated from said first device region;

a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;

a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region and electrically connected to said body;

wherein said top gate and semiconductor body operable as a top and bottom gate respectively of a JFET channel formed by said drift region;

said top gate having a surface area doping density such that it becomes totally depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

6. A semiconductor device as claimed in claim 5 wherein said first device region is a drain of a lateral drift region MOS device;

said semiconductor device further comprising an MOS gate located over said separation zone and overlapping a portion of said drift region.

7. A semiconductor device as claimed in claim 5 wherein said first device region is a collector of a lateral bipolar transistor and wherein said separation zone comprises an emitter shield region of said first conductivity type.

8. A semiconductor device as claimed in claim 5 wherein said drift region and top gate are in contact with said first device region about the entire periphery of said first device region.

9. A lateral MOS structure comprising a semiconductor body of a first conductivity type, source and drain regions of a second conductivity type forming respective source and drain junctions with said body, and a drift region of said second conductivity type, said drift region forming a JFET channel in said body controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift regions becomes depleted, and

a top gate of said first conductivity type formed in said drift region and being electrically connected to said body, said top gate having a surface area doping density such that it becomes totally depleted below a body to drain voltage at which said drift region becomes depleted.

10. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is laterally spaced from said drain.

11. A lateral MOS structure as claimed in claim 9 wherein:

a body contact of said first conductivity type is formed in said body and said top gate overlaps said body contact, said body contact having an impurity concentration higher than the impurity concentration of said drift region.

12. A lateral MOS structure as claimed in claim 9 wherein:

said drift region and said top gate extend laterally around the entire surface intersection of the drain to body junction to reduce the surface field and thereby increase breakdown voltage of the drain to body junction.

13. A lateral MOS structure as claimed in claim 9 wherein:

said top gate totally depletes below a body to drain voltage at which said drift region totally depletes.

14. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is formed by an ion implant, and said top gate has a tapered peripheral edge.

15. A lateral MOS structure as claimed in claim 14 wherein:

said drift region is formed by an ion implant and said drift region has a tapered peripheral edge.

16. A diode structure comprising:

a first semiconductor body of a first conductivity type contained within a semiconductor region of a second conductivity type and forming a diode junction therewith, said semiconductor region having a first dopant concentration,

a second body of said first conductivity type contained within said semiconductor region and having a second dopant concentration greater than said first dopant concentration, said second body surrounding the lateral perimeter of said first body and abutting said first body;

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, and

a top gate of said second conductivity type formed within said second body and being electrically connected to said first semiconductor region, said top gate having a dopant concentration such that upon application of said reverse bias, said top gate becomes totally depleted before said second body becomes depleted.

17. In a diode structure as claimed in claim 16, the improvement compcising:

a tapered peripheral edge for said top gate.

18. In a diode structure as claimed in claim 17, the improvement comprising:

forming said tapered peripheral edge by implanting said top gate using an implant mask with a tapered edge.

19. In a diode structure as claimed in claim 16, the improvement comprising:

forming a tapered peripheral edge for said second body by implanting said second body using an implant mask with a tapered edge.

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EXHIBIT B

United States Patent [19]
Eklund

[11] **Patent Number: 4,811,075**
[45] **Date of Patent: Mar. 7, 1989**

[54] **HIGH VOLTAGE MOS TRANSISTORS**

[75] Inventor: Klas H. Eklund, Los Gatos, Calif.

[73] Assignee: Power Integrations, Inc., Mountain View, Calif.

[21] Appl. No.: 41,994

[22] Filed: Apr. 24, 1987

[51] Int. Cl.[4] H01L 27/02; H01L 29/78; H01L 29/80

[52] U.S. Cl. 357/46; 357/22; 357/23.4; 357/23.8

[58] Field of Search 357/23.8, 23.4, 46, 357/22

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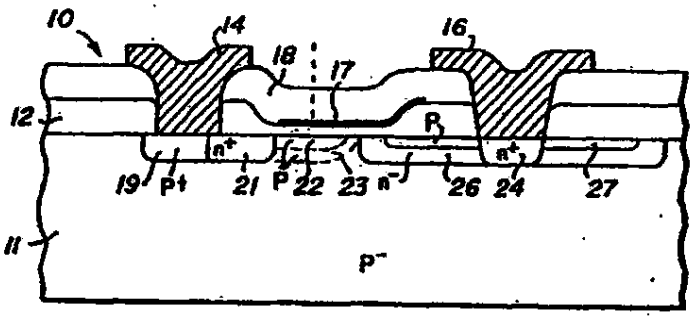
Primary Examiner—Andrew J. James
Assistant Examiner—Jerome Jackson
Attorney, Agent, or Firm—Thomas E. Schatzel

[57] ABSTRACT

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

7 Claims, 2 Drawing Sheets



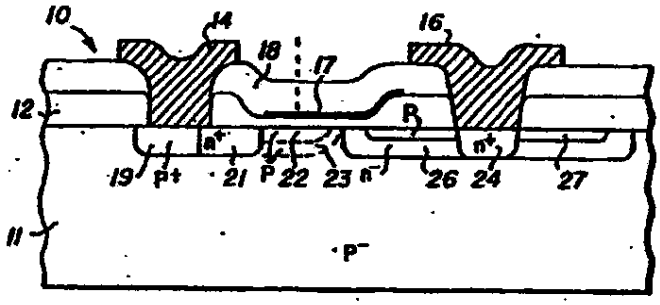


Fig_1

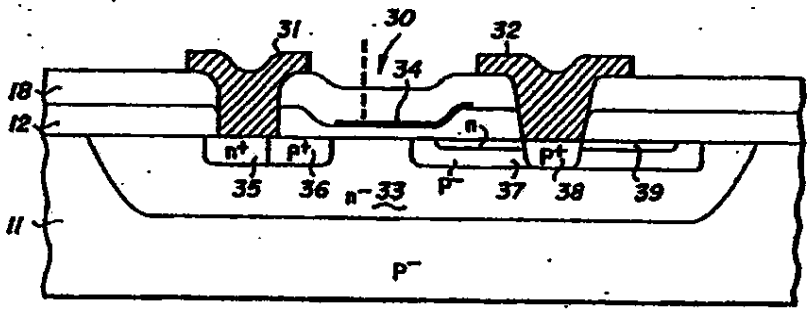


Fig_2

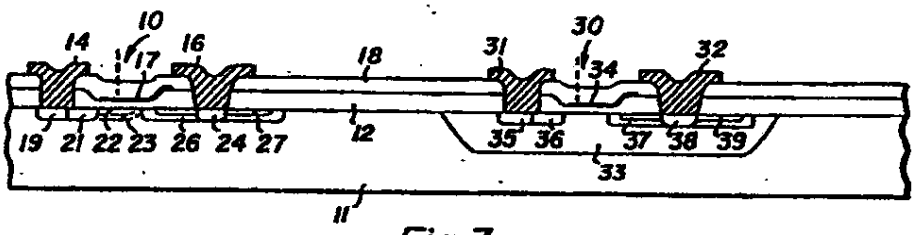
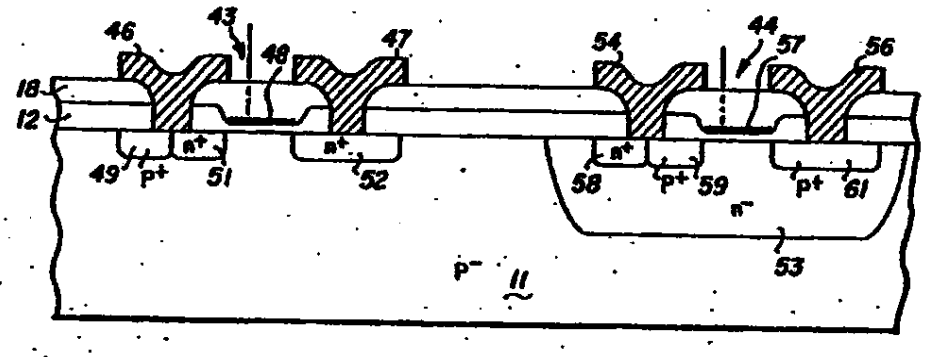


Fig_3


46
43
48
47
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44
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12
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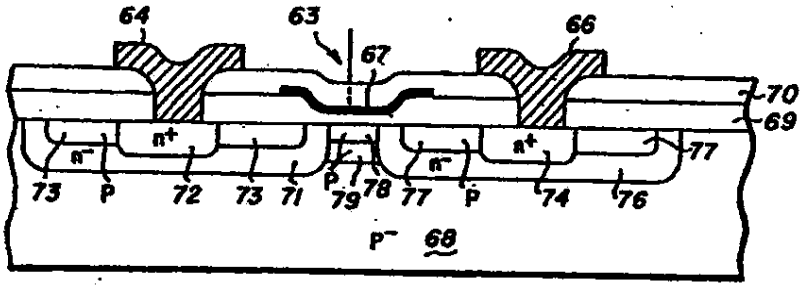
Fig_4


64
63
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n+
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Fig_5

HIGH VOLTAGE MOS TRANSISTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on} \times A$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on} \times A$ is typically 10-15 Ω mm^2. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 Ω mm^2, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on} \times A$, of about 2.0 Ω mm^2.

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about 2.0 Ω mm^2.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 2 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p^+ material and a pocket 21 of n^+ material are diffused into the p^- substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n^+ material is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1\times10^{12}/cm^2$ to around $2\times10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of 5×10^{16}-$1\times10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1\times10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, R_{on} x A, of about 2.0 Ω mm² for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10-15 Ω mm², while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3-4 Ω mm².

With reference to FIG. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n^+ type material and a pocket 36 of p^+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from beneath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p^+ drain contact pocket 38 and the n-well.

Looking now at FIG. 3, an n-channel transistor 10, similar to that shown in FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. 1 and 2, no further description is considered necessary.

As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in FIG. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p^+ pocket 49 and an n^+ pocket 51 are provided in the p^- substrate beneath the source contact. The n^+ pocket extends to beneath the gate. An n^+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n^+ pocket 58 and a p^+ pocket 59 are provided in the n-well beneath the source contact and a p^+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends therabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n^+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dioxide layer thereabove. Beneath the drain contact is an n^+ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 Ωmm^2. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions, said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a depth of one micron or less.

3. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a doping density higher than $5 \times 10^{16}/cm^3$ so that the mobility starts to degrade.

4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.

6. The combination of claim 5 further including,
- a complementary high voltage MOS transistor, and
- a complementary low voltage CMOS implemented device on the same chip and isolated from each other.

7. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface,
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,

said top layer and said substrate being subject to application of a reverse-bias voltage,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

* * * * *

EXHIBIT C

REDACTED

EXHIBIT D

REDACTED

EXHIBIT E

REDACTED

EXHIBIT F

de Blank, Bas

From: Michael Headley [Headley@fr.com]
Sent: Wednesday, October 26, 2005 2:54 PM
To: de Blank, Bas
Subject: Re: PI-Fairchild: discovery/claim construction status and supplemental interrogatories

Bas,

We need to discuss a number of outstanding issues, including the schedule for depositions of several Fairchild employees, outstanding production Fairchild owes Power Integrations, errors in the joint claim construction chart you provided last week, the status of Fairchild's supplemental privilege log, and the like. Let me know if you are available later this afternoon or tomorrow afternoon after the deposition of Mr. Brunnberg to discuss these issues, or e-mail me if you have further word before that time with respect to any of the various issues we've been discussing. I address several of outstanding issues below.

With respect to the issue of supplemental responses to Fairchild's interrogatories, Power Integrations will supplement its responses to Interrogatory Nos. 22, 33, 34, 37, 40, and 47 (in addition to the responses called out in the Court's recent order). Power Integrations will not supplement its response to Interrogatory No. 48 without further justification than your repeated demand.

It appears as though Mr. Lelieur is available to reschedule his deposition on November 29 or 30. I believe the 30th is better for him, but let me know if either of these days works on your end so that I can confirm with him as soon as possible. This schedule will provide plenty of time between the supplementing of Power Integrations' interrogatories and the deposition to alleviate the concerns you had raised with respect to the proximity of two events.

With respect to the issue you raised regarding Power Integrations' Second Supplemental Response to Interrogatory No. 8, Power Integrations does not intend to rely on the testimony of Leif Lund with respect to the invention of the '075 patent. Although I disagree with your contention that the supplemental response provides a basis for further deposition of Mr. Lund, I believe my response obviates the concern you raised with respect to this issue. Let me know if it does not.

Sincerely,

Michael R. Headley
Fish & Richardson P.C.
500 Arguello St., Suite 500
Redwood City, CA 94063-1526
(650) 839-5139 (direct)
(650) 839-5071 (fax)

EXHIBIT G

REDACTED

EXHIBIT H

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EXHIBIT I

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EXHIBIT J

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EXHIBIT K

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EXHIBIT L

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EXHIBIT M

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EXHIBIT N

United States Patent [19]

Sirsi

[11] **4,283,236**

[45] **Aug. 11, 1981**

[54] **METHOD OF FABRICATING LATERAL PNP TRANSISTORS UTILIZING SELECTIVE DIFFUSION AND COUNTER DOPING**

[75] Inventor: **Ramesh M. Sirsi, Indialantic, Fla.**

[73] Assignee: **Harris Corporation, Melbourne, Fla.**

[21] Appl. No.: **77,234**

[22] Filed: **Sep. 19, 1979**

[51] Int. Cl.³ **H01L 21/22; H01L 21/31**

[52] U.S. Cl. **148/187; 29/578; 148/1.5; 148/175; 357/35; 357/44; 357/89; 357/92**

[58] Field of Search **148/1.5, 175, 187; 29/578; 357/34, 35, 44, 46, 89, 91, 92**

[56] **References Cited**

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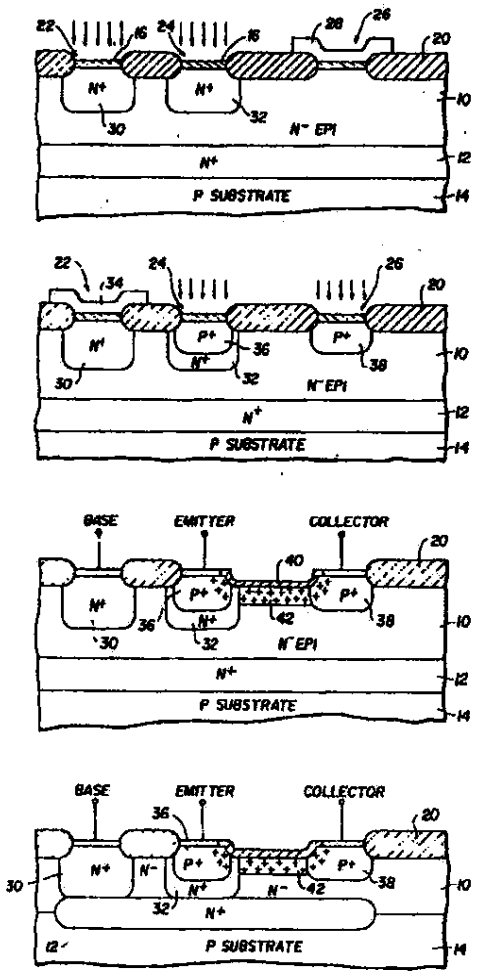
Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Leitner, Palan, Martin & Bernstein

[57] **ABSTRACT**

A lateral PNP transistor is formed by diffusing N type impurities into an N type layer to form base contact region and base region, diffusing P type impurities into the N base region and N layer to form emitter and collector regions respectively, and counter doping the layer area between the N base region and the collector region. The counter doping is performed through a non-critical mask aperture extending between the emitter and collector regions.

11 Claims, 8 Drawing Figures



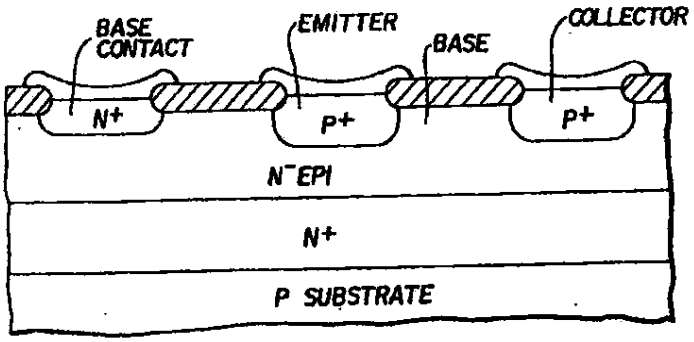


FIG. 1
PRIOR ART

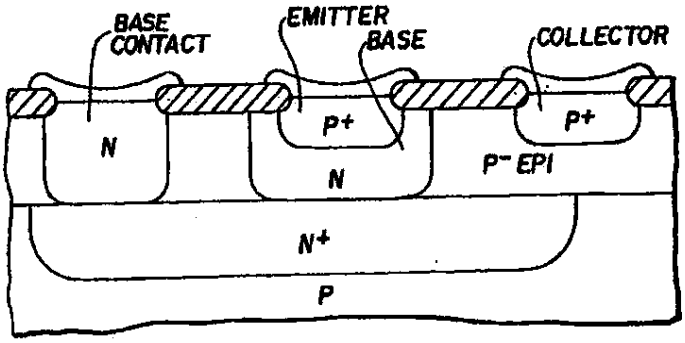


FIG. 2
PRIOR ART

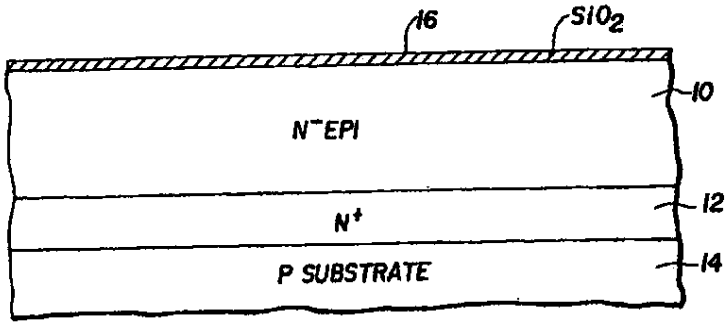


FIG. 3

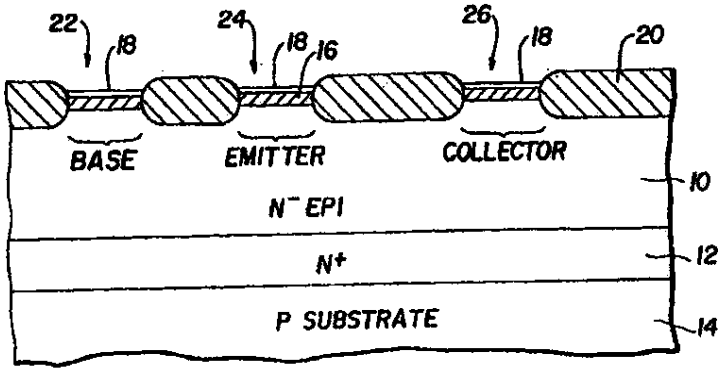


FIG. 4

FIG.5

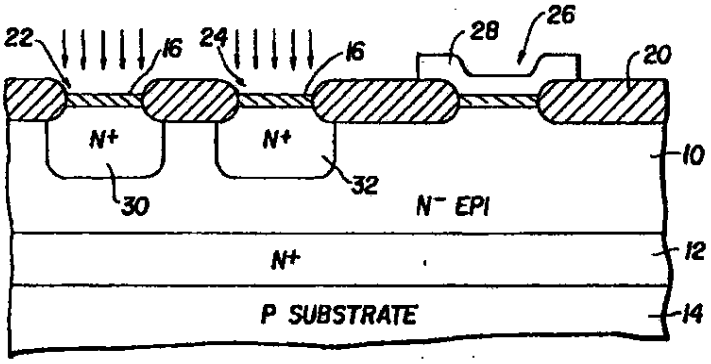


FIG.6

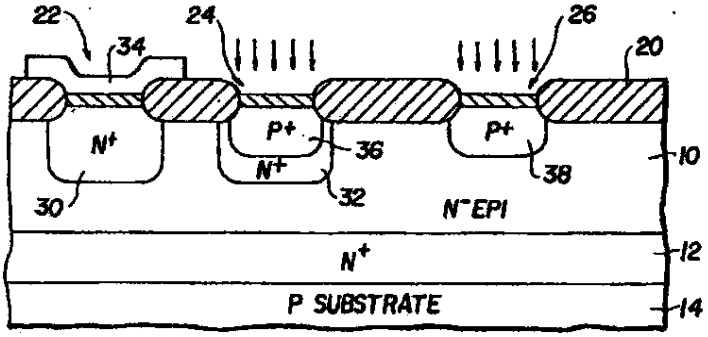


FIG.7

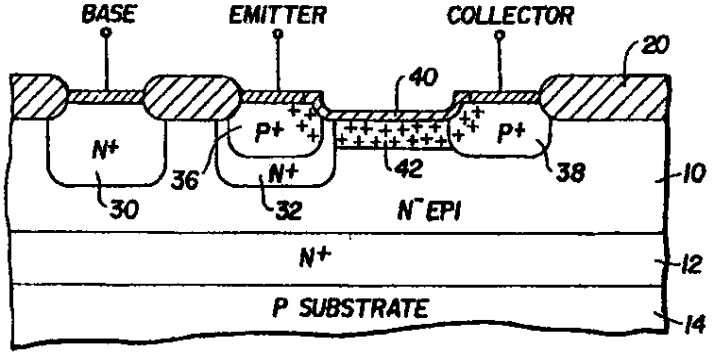
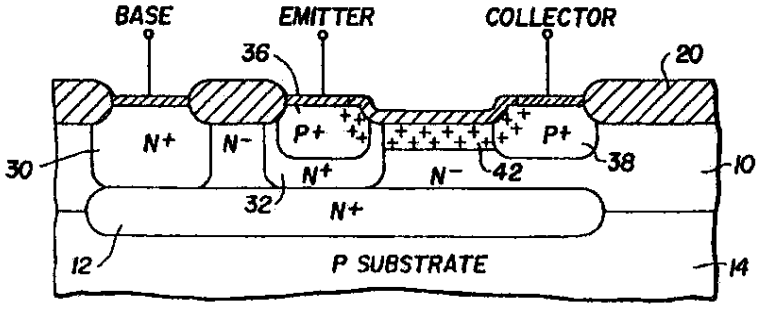


FIG.8



METHOD OF FABRICATING LATERAL PNP TRANSISTORS UTILIZING SELECTIVE DIFFUSION AND COUNTER DOPING

BACKGROUND OF THE INVENTION

The present invention relates generally to lateral bipolar transistors and more specifically to an improved double diffused PNP lateral bipolar transistor.

Conventional lateral PNP bipolar transistors are generally fabricated by simultaneously diffusing P type collector and emitter regions side by side in an N epitaxial base region during the P base diffusion cycle of the vertical NPN transistors. This structure is illustrated in FIG. 1. The main problems in achieving high performance lateral PNP transistors using this scheme are that the distance between the emitter and collector regions cannot be reduced anymore than the limits of the photolithographic process. Thus, there is a technological limitation to the minimum base which is achievable by this method. This limitation correctly influences the performance characters of the device. Another difficulty is that the N− region which is common to the PNP and NPN devices cannot be independently optimized. Further the uniformity of the N− epitaxial base region does not contribute to enhancing carrier transport across the base region.

To improve the charcateristics of the lateral PNP transistor, a double-diffused technique was developed. This technique basically involved diffusing N type impurities through an aperture into a P epitaxial region to form the base region and subsequently diffusing P type impurities through the same aperture to form the emitter region. Thus, the base width would be the difference between the P emitter diffusion and the N base diffusion. The resulting structure is specifically shown in FIG. 2. This technique is specifically described in U.S. Pat. No. 3,766,446 for an NPN lateral transistor. A doubly-diffused lateral PNP transistor not using this same aperture but achieving the same results is illustrated in U.S. Pat. No. 3,873,989.

The prior art structure of FIG. 2 although reducing the base width, results in a structure which is incompatible with the formation of other elements in an integrated circuit. This results because of the use of the P− epitaxial region which prevents readable formation of vertical NPN devices. Similarly, it should be noted that the P− epitaxial region which forms the bulk collector between the P+ collector contact region and the N base region contributes to the series collector resistance which in turn influences both the frequency response and saturation voltage for the bipolar transistor.

Thus, there exists a need for a method of fabricating a lateral PNP transistor which is compatible with the formation of other devices in an integrated circuit as well as providing improved frequency response and voltage saturation.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method of fabricating PNP lateral transistors in an N epitaxial layer so as to make the device formation compatible with other elements in an integrated circuit.

A further object of the present invention is to provide a method of fabricating a lateral PNP transistor which will enhance a carrier transportation across the base region.

A still further object of the present invention is to provide a fabrication method which allows independent adjustment of frequency response and saturation voltage of a PNP lateral transistor.

An even further object of the present invention is to provide a method of fabricating a PNP bipolar transistor which enhances the emitter injection efficiency.

A still even further object of the present invention is to provide a method of fabricating a PNP lateral transistor wherein the characteristics are substantially independent of the N epitaxial layer in which it is formed.

These and other objects, advantages, and novel features of the present invention are achieved by the following process.

A masked layer is formed on an N epitaxial layer having base contact, emitter, and collector apertures, therein. N type impurities are introduced through the base contact and emitter regions to form a base contact and base regions having a higher impurity concentration than the N epitaxial layer. P type impurities are then introduced through the emitter and collector apertures to form an emitter region in the N base region and a collector region in the N epitaxial layer. The masking material is then removed from between the emitter aperture and the collector aperture. P type impurities are then introduced through the enlarged aperture to counter dope the N epitaxial area between the base region and the collector region sufficiently to convert this area to P conductivity type without converting the N diffused base region. Metal contacts can then be made to the appropriate regions. The masked layer may be formed by preferentially oxidizing the substrate to form thick oxide masking layer and thin oxide regions in the apertures. The impurities may be introduced by ion implantation. By forming the N base region by diffusion into an N epitaxial layer, a graded base structure is produced. The electric field created by the gradient of impurities in the base region enhances the transporation of carriers across the lateral base region and thereby improving frequency performance of the device. The counter doping can be adjusted to individually tailor the frequency response and saturation voltage of the device independent of the epitaxial layer. By using the counter doping step, a non-critical step for this mask may be used since the impurities introduced during the counter doping step will have no effect on the emitter and collector regions except to enhance the emitter efficiency and will have minimal effect on the high impurity diffused base region.

Other objects, advantages and novel features of the present invention will become evident when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of PNP lateral transistor of the prior art.

FIG. 2 is a cross-sectional view of another PNP lateral transistor of the prior art.

FIGS. 3 through 7 are cross-sectional views of a PNP lateral transistor at various states of fabrication according to the principles of the present invention.

FIG. 8 is a cross-sectional view of another PNP lateral transistor incorporating the principles of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of fabrication according the principles of the present invention, as illustrated in FIG. 3, begins with a wafer having an N− epitaxial region 10 of an impurity concentration of 10^{15} and a bulk resistance of 5 ohms-centimeters formed on an N+ layer or buried region 12 having a sheet resistance of 15 ohms per square which is formed on a P substrate 14 which has a bulk resistance of 1 to 2 ohm-centimeters. The top surface of the N epitaxial layer 10 is covered by a thin oxide layer 16 of for example 800 angstroms thickness. To form a mask having apertures for the base contact, emitter, and collector regions, the thin oxide layer 16 is covered by an oxidation inhibiting layer, for example silicon nitride, and delineated leaving the silicon nitride layer only over that portion of the oxide layer which are to become the apertures of the mask. The wafer is then oxidized resulting in a thick oxide layer 20 having base contact aperture 22, emitter aperture 24 and collector aperture 26 therein. The resulting structure is illustrated in FIG. 4. The silicon nitride or oxidation inhibiting layer is then removed from the apertures and the wafer is ready for region formation.

Although the masking layer has been described as being formed by the growth of a thick oxide layer and a thin oxide layer, obviously, other methods may be used to form the masking layer. These methods may include forming an initially thick oxide layer and etching to form the apertures. As will be noted hereafter, the preferred method is to introduce impurities by an implantation and, thus, it is desirable to have a thin oxide layer in the apertures in the mask to protect the N epitaxial layer surface. The differential oxidation technique results economically and proficiently in the combined thin and thick oxide layers although the thin oxide regions may be formed after etching a thick oxide region.

The first impurites to be introuded into the N epitaxial region 10 are N type impurities, for example phosphorous, to produce a base contact and base regions. Since this diffusion is to take place only through base contact aperture 22 and emitter aperture 24, a mask must be formed over the collector aperture 26. This mask is formed by applying a metal layer and delineating the same. The resulting mask 28 is illustrated in FIG. 5. Impurities may be introduced by deposition and diffusion or by ion implantation. The resulting base contact region 30 and base region 32 have an impurity concentration of 10^{17} carriers/cm^3 and a depth of 2 microns.

The next impurity introduction is to be through the emitter and collector apertures 24 and 26, respectively to form the emitter and collector regions. Thus, the base contact aperture 22 must be masked. As for the previous impurity introduction step, a layer of metal is applied and delineated to produce a resulting mask 34 in base contact aperture 22, as illustrated in FIG. 6. P type impurities, for example, boron, are introduced through emitter aperture 26 and collector aperture 28 to form emitter region 36 in the base region 32 and collector region 38 in the epitaxial layer 10. The emitter region 36 and collector region 38 have an impurity concentration of 10^{19} carriers/cm^3 and a depth of approximately 1 to 2 microns. As with the previously impurity introduction step, the impurities may be introduced by deposition and diffusion or preferably by ion implantation and diffusion.

Finally, a portion of the thick oxide layer 20 between the emitter and collector apertures 26 and 28 is etched to form a substantially thin oxide region 40 as illustrated in FIG. 7. The wafer is then subjected to a non-critical or non-selective P type impurities introduction so as to counter dope the area of the N epitaxial region 10 between the collector region 38 and the base region 32. Using ion implantation for example, the dope N level have a dosage of 2.0×10^{11} at an implant energy of 60 KeV is sufficient to convert the region of the N epitaxial layer 10 between the collector 38 and the emitter 32 to a P type region 42 having impurity concentration of 10^{16} carriers/cm^3 and a depth of 0.6 microns. This counter doping step is insufficient to convert the highly doped N+ base contact region 30 and base region 32 which are not masked during this step. The additional P type impurities enhance the emitter injection efficiency thus improves the current gain in the lateral direction.

The counter doping step allows the use of an N− epitaxial layer as the region in which the PNP lateral transistor is formed. Thus, the process is compatible with the formation of other devices in other portions of the N epitaxial layer. Similarly, the counter doping allows individual tailoring of the collector resistance, and thus adjustment of the frequency response and the saturation voltage. Similarly, by the selection of the impurity concentration and depth of the ion implantation of the counter dope region 42, the grade of the impurity profile of the N+ base region 32 and epitaxial base portion 10 can be individually tailored to define the degree of enhancement of a transportation of carriers across the lateral base region so as to improve the frequency performance of the device. The counter doping step in the formation of counterdoped region 42 achieves the same sub-micron base width of the double-diffused lateral transistors of the prior art while allowing tailoring of the bulk resistance of this portion.

The process is completed by removing the thin oxide layer and forming metal contacts. These contacts are formed by the application of, for example, a metal layer and delineation of the metal layer to form the contacts and innerconnects.

As illustrated in FIG. 8, the process of the present invention may also be used for a lateral PNP transistor with a substantially reduced series base resistance. The above process is initially modified to form the buried N+ region 12 and limit the thickness of the epitaxial layer 10. During the subsequent processing steps to form base contact 30 and base region 32, the down diffusing base contact 30 and base region 32 mate with the up diffusing buried region 12 in the limited thickness epitaxial layer 10. This base structure will substantially eliminate the flow of base current through the N− epitaxial region 10 and thus reduce the series base resistance considerably.

It is evident from the description of the preferred embodiments, that the objects of the invention are attained in that a process is provided which results in an improved lateral PNP transistor. Although the invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation. The spirit and scope of this invention is to be limited only by the terms of the appended claims.

What is claimed:

1. A method of fabricating lateral PNP transistors comprising:

introducing N type impurities into a low impurity concentration N type base region to form high impurity concentration N type base and base contact regions;

introducing P type impurities into said low impurity concentration base region to form P type collector region and into said high impurity concentration base region to form P type emitter region; and

introducing P type impurities into the region between said collector and emitter regions of sufficient concentration to counter dope the low impurity concentration base region between said collector region and said high impurity concentration base region without converting said high impurity concentration base region.

2. The method according to claim 1 wherein said P type impurities of the last mentioned step are introduced through a noncritical mask having an aperture over said base regions between said collector and emitter regions and portions of said collector and emitter regions.

3. The method according to claim 1 including forming a thick oxide layer on said low impurity concentration base region having base contact, emitter and collector region apertures in said thick layer, and subsequently introducing said impurities through said apertures.

4. The method according to claim 3 wherein said N type impurities are introduced through said base contact and emitter apertures, and said first mentioned P type impurities are introduced through said emitter and collector apertures.

5. The method according to claim 4 including removing portions of said thick oxide layer between said emitter and collector apertures between said first and second P type impurity introducing steps.

6. The method according to claim 3 wherein said apertures have thin oxide regions compared to said thick oxide layer and said impurities are introduced by ion implantation through said thin oxide regions with said thick oxide layer forming an implantation mask.

7. A method of fabricating lateral PNP transistors comprising:

forming a mask layer on an N type with base contact, emitter and collector apertures in said mask layer;

introducing N type impurities through said base contact and emitter apertures to form a base contact region and base region of higher impurity concentration than said layer;

introducing P type impurities through said emitter and collector apertures to form an emitter region in said base region and collector region in said layer;

removing portion of said mask layer between said emitter and collector apertures; and

introducing P type impurties into the region between said emitter and collector regions of sufficient concentration to counter dope the portion of said layer between said collector region and said base region without converting said base region.

8. The method according to claim 7 wherein said impurities are introduced by ion implantation; and said collector aperture is masked during said N type impurity ion implantation and said base contact aperture is masked during the first P type impurity ion implanatation.

9. The method according to claim 8 wherein the base contact, emitter and collector apertures are exposed during the second P type impurity ion implantation.

10. The method according to claim 9 wherein said apertures are masked by metal formed in said apertures.

11. The method according to claim 10 wherein forming said mask layer includes forming a thin oxide layer on said N type layer, forming oxidation inhibiting mask on said thin oxide layer to define said apertures and oxidizing said exposed thin oxide layer to form a thick oxide layer with thin oxide in said apertures.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,283,236

DATED : August 11, 1981

INVENTOR(S) : Ramesh M. Sirsi

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in the abstract:

Line 2, delete "inpurities" and insert --impurities--

Signed and Sealed this

Seventh Day of December 1982

[SEAL]

Attest:

GERALD J. MOSSINGHOFF

Attesting Officer Commissioner of Patents and Trademarks

CERTIFICATE OF SERVICE

I hereby certify that on the 23rd day of March, 2006, the attached **REDACTED PUBLIC VERSION OF OPENING BRIEF IN SUPPORT OF DEFENDANTS' MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF CLAIMS 1 AND 5 OF U.S. PATENT NO. 4,811,075** was served upon the below-named counsel of record at the address and in the manner indicated:

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